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Joaquin Santander^a, Iñigo Martin-Fernandez^a, Carlos Carbonell^a, Alex Rodríguez-Iglesias^a, Laura Fuentes-Rodríguez^a, Marta Fernández-Regúlez^a, Llibertat Abad^a, Aitor F. Lopeandia^{b,c}, Arindom Chatterjee^d, Nini Pryds^d, Luis Fonseca^a, and Marc Salleras^{a*}

^a*Institute of Microelectronics of Barcelona (IMB-CNM-CSIC), 08193 Bellaterra, Spain.*

^b*Physics Department, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain.*

^c*GTNAM at Institut Català de Nanociència i Nanotecnologia (ICN2), 08193 Bellaterra, Spain.*

^d*Department of Energy Conversion and Storage, Technical University of Denmark, 2800 Kgs Lyngby, Denmark.*

*marc.salleras@csic.es

A novel approach to micro-fabricated thermoelectric generators with SrTiO₃

The growing demand for autonomous, sustainable, and delocalized power sources for low-power-consuming electronic devices is driving a significant research effort on energy harvesting technologies. Among these, micro-thermoelectric generators (μ TEGs) emerge as an appealing solution because of the abundance of residual latent heat sources. This paper proposes an approach to combine high-performance thermoelectric oxides with Si-based μ TEGs, leveraging the miniaturization and high-density integration of CMOS-like technologies. The approach is applied to the integration of niobium doped strontium titanate (Nb:STO) thin films on Si-based planar μ TEG structures. The Nb:STO-based μ TEG achieves a specific power density $\Gamma = 0.36 \text{ nW} \cdot \text{cm}^{-2} \cdot \text{K}^{-2}$ under controlled temperature gradients, which is below state-of-the-art performance probably due to lower electrical conductivity from polycrystalline growth. When the chips were tested under realistic operating conditions—placed on a hot surface at 175 °C—a maximum power output of $P = 0.07 \text{ nW}$ was obtained. Nonetheless, by implementing a technological solution for thermal dissipation, the temperature gradient across the thermoelectric material improved by a factor of 110, resulting in a significantly higher extracted power of $P = 7.75 \text{ nW}$.

Keywords: thermoelectric; micro-thermoelectric generator; thin-films; SrTiO₃; IoT;

Subject classification codes: 105; 210; 306; 206; 208.

Introduction

Thermal sources such as automotive engines, industrial processes, and home heating generate enormous amounts of waste heat [1] that could be converted into useful energy if efficient low-temperature thermal energy harvesters were available [2–4]. In this frame, thermoelectric generators (TEGs), solid state devices that convert heat (some temperature difference) into electric energy, become an attractive solution to self-powered electronic systems and as a sustainable alternative to conventional batteries, reducing the reliance on critical raw materials (CRM) in energy-related technologies.

TEGs are of particular interest to power devices that are delocalised, or whenever accessibility to replace the batteries is challenging, for example, in Internet of Things (IoT) networks and harsh environments, such as industrial reactors, power stations and volcanoes [5–10].

The thermoelectric efficiency of a material is expressed by the dimensionless figure of merit zT :

$$zT = \frac{S^2 \sigma}{\kappa} T \quad (1)$$

where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity, and T is the temperature. The materials with the highest zT in the low and intermediate temperature ranges (from 300 K to 600 K [9]) are typically based on scarce and toxic elements, such as tellurium and lead. In addition, the fabrication of the related TEG faces limitations for mass production and miniaturization that hinder integration and deployment with mass-produced electronic devices like the nodes in IoT networks [11]. Consequently, current research in thermoelectric materials focuses on balancing performance with sustainability by using more abundant and low-toxicity materials such as Half-Heusler alloys, lead-free chalcogenides, silicides, perovskites, and organic thermoelectrics [12], on novel technological solutions for the TEGs to better conform to the heat surfaces to optimise thermal efficiency at the device level and to unlock new uses, and on enabling mass production. In the latter case, TEG technologies based on a modest zT material like Si benefit from miniaturisation, scalability and efficiency in the use of materials provided by semiconductor micro- and nanotechnologies (MNTs) [10,13–15]. MNTs enable optimising the architecture of the micro-TEG (μ TEG) and implementing thermal engineering to maximise the temperature difference across the thermoelectric material that critically determine the device performance, ZT [16–19]. It

has been demonstrated how this approach can provide output powers well within the range of IoT needs [20–23].

The thermoelectric efficiency of a TEG is expressed by the dimensionless figure of merit ZT :

$$ZT = \frac{S^2 G}{K} T \quad (2)$$

where G is the electrical conductance, and K is the thermal conductance, and T is the temperature. Here, it needs to be noted that ZT [17] is critically determined by the device architecture and thermal engineering at device level, which serve at maximizing the temperature difference across the thermoelectric material.

In this work, we demonstrate a multiscale approach to explore the integration of novel thin-film thermoelectric materials with Si-based micro-electromechanical systems (MEMS) technologies, to evaluate the impact of the related planar μ TEG architecture (dimensions and shape of the active material) and device thermal management (heat dissipator integration with >100x extracted power improvement), and to benchmark their performance. As a proof-of-concept, 6 mol% niobium-doped strontium titanate (Nb:STO) thin films are patterned on square-shaped $\text{SiO}_2/\text{Si}_3\text{N}_4$ planar membrane devices, a heat dissipator is implemented, and the performance of the related μ TEG is evaluated.

Nb:STO thin films and integration

SrTiO_3 (STO)-based thin films offer a large variety of physical properties such as metal-insulator transition, ferro-, piezo-, pyro- and flexo-electricity, high thermopower, ferromagnetism, superconductivity, high electron mobility at low temperatures and resistive switching [24–27] making STO the “work horse” of many oxide-based devices. It is

well know that Nb-doping in Ti-site of pristine insulating SrTiO₃ (Nb:STO) makes it an n-type conductor, which exhibits good thermoelectric properties [28,29]. The highest power factor ($PF = \sigma \cdot S^2$) of $\approx 2.6 \text{ mW} \cdot \text{m}^{-1} \cdot \text{K}^{-2}$ was achieved near room temperature for STO films which are doped between 5–8% Nb [30,31].

In this work, Nb:STO thin films were grown by Pulsed Laser Deposition (PLD) with the same conditions previously reported in [32]. Structural analysis of the as-grown films was carried out by standard X-ray diffraction in a $2\theta/\omega$ configuration using Panalytical X'pert pro-MRD diffractometer. The thicknesses of the films were determined by deposition time calibration combined with using physical etching (RIE) and profilometer.

μ TEG Device Architecture

The μ TEG is a planar device that induces a temperature gradient across the thermoelectric material lying on a membrane (Figure 1). A doped silicon (d-Si) platform in the central part of the membrane hosts a metal serpentine that operates as a heater and thermometer, and homogenises the temperature. The serpentine is connected with a 4-wire scheme (force wires: F⁺ and F⁻, and sense wires: S⁺ and S⁻) to avoid contact resistance during resistance measurement. Current collectors contact the thermoelectric material at the edge of the d-Si platform (internal collector) and over the bulk silicon (external collector). The external current collector has two metal tracks that connect at the external contact pads. The chip hosts five devices (D1 to D5) with geometrical variations in the lateral length of the internal platform (w) and in the gap between the platform and the bulk Si (g) (Table 1).

The architecture of the devices allows the evaluation of the performance of the μ TEG in two different modes. In *test* mode, a thermal gradient is generated across the

TE material by forcing a controlled current to the serpentine on the d-Si platform, which acts as a heater, and maintaining the bulk Si at room temperature. In *harvest* mode, the thermal gradient is naturally generated by placing the Printed Circuit Board (PCB) where the chip is mounted on a hotplate. The serpentine on the d-Si platform is used as a thermometer to evaluate the thermal gradient. The current on the thermometer is chosen to avoid Joule heating. This *harvest* mode is closer to an actual application, while the *test* mode allows evaluating the maximum possible performance under a given thermal gradient. In both cases, the heater can be used as a thermometer once its Temperature Coefficient of Resistance (*TCR*) has been characterized.

Fabrication

The micro-fabrication of the μ TEG is divided into two blocks. The first block comprises the main process steps to fabricate the platforms. It is performed at a wafer-scale level. The second block focuses on the integration of the thermoelectric Nb:STO thin film into the μ TEG, and it is completed at chip-level because of sample size limitations at the PLD system.

Within the first block, the Si is selectively doped with boron to concentrations in the order of 10^{20} at cm^{-3} to define the d-Si platforms and the contour of the membrane areas. Next, 100 nm SiO_2 are thermally grown and 300 nm Si_3N_4 are deposited by Low Pressure Chemical Vapor Deposition (LPCVD) on both sides of the wafer. This bilayer will form the membrane where the TE oxide material is to be deposited. Then, windows are patterned on the backside of the wafers by optical lithography and RIE, and a partial KOH etching of the Si is performed to leave 150 μm of bulk Si under the platform for structural robustness. At this point, the wafer is diced into chips.

Within the second block, the Nb:STO thermoelectric layer is first deposited by PLD. The thickness of the Nb:STO thin film layer ($t_{Nb:STO}$) on the chip reported here is 149 nm. Then, the Nb:STO thin film is patterned by optical lithography followed by a dry etching process with Ar plasma. Next, a 200 nm thick SiO₂ layer is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) to serve as an interlevel dielectric and contacts to the Nb:STO are opened by optical lithography and wet etching. The metal layer is defined by an optical lithography, sputtering of 30 nm of Ti plus 200 nm of W and a lift-off process. Last, the exposed Si on the backside is chemically etched with KOH to release the membranes. (see Fig. S1 with steps detailing fabrication process).

The chip includes a set of electrical test structures (see Fig. S2) to evaluate electrical technological parameters like the sheet resistance (Van der Pauw test structures) and the contact resistance between conducting layers (Kelvin test structure). The electrical conductivity is calculated based on the sheet resistance measurements and the thickness of the layer ($\sigma = 1/(R_{\square} \cdot t)$). The sheet resistance obtained for the Nb:STO is $R_{\square, Nb:STO} = 49 \text{ k}\Omega$ and the calculated electrical conductivity is $\sigma_{Nb:STO} = 1.37 \text{ }\Omega^{-1} \cdot \text{cm}^{-1}$. The contact resistance between metal and Nb:STO is $R_c = 6.8 \cdot 10^{-3} \text{ }\Omega \cdot \text{cm}^2$ on a $20 \times 20 \text{ }\mu\text{m}^2$ contact area (see Table S1).

Characterization

Before evaluating the performance of the device in *test* or *harvest* modes, the heaters in the centre of each platform need to be calibrated by measuring their temperature coefficient of resistance (*TCR*) to use them as thermometers. To calculate the thermal gradient seen by the thermoelectric material, the temperature of the bulk Si was measured on

similar setups. It was determined to be the same temperature as that of the bottom PCB within ± 0.5 °C.

TCR measurements were made on a PCB with the wire-bonded device inside an oven. Before any measurement was made, the highest possible current at which the heater temperature remained stable and unaffected by Joule heating was determined. As an additional test, the open circuit output voltage of the device, V_{OC} , was also evaluated at different currents on the heater to validate that they would not generate a temperature gradient. It was found that 50 μ A was the highest current that did not generate a measurable V_{OC} in any of the devices on the chip. The resistance of the heaters was measured with this current at six different temperatures, ranging from room temperature (RT) to 175 °C. Then, the *TCR* value for each of the heaters can be obtained using equation (3):

$$R = R_0 \cdot \left(1 + TCR \cdot (T - T_0) \right) \quad (3)$$

where R_0 is the value of the resistance at $T = T_0$, and T_0 is the room temperature.

In addition to the thermoelectric characterization, a dedicated chip was used to measure the in-plane thermal conductivity by the 3ω Völklein method [17]. The obtained value for a 25 nm thick sample of Nb:STO was $k_{Nb:STO} = 3.118 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$ at room temperature. The obtained value is lower than bulk STO due to phonon boundary scattering in thin films and the additional point-defect scattering introduced by Nb doping,

Device performance and discussion

The device performance was evaluated by applying current to the heater (*test* mode). Adjusting the current makes it possible to control the temperature of the central part of the membrane, while the temperature of the cold side was measured with a thermocou-

ple on the bottom of the PCB. For each ΔT across the device, a performance plot (voltage and power vs. current) was obtained. Figure 2 a-e) shows the performance plots for the five devices on the chip at different ΔT . The maximum power (P_{max}) obtained was for the D4 device with a total of 53.26 nW at $\Delta T = 152$ K. The maximum power density ($P_{dens} = P_{max}/Area$) resulted in $8.32 \mu W \cdot cm^{-2}$. To compare with other devices at different temperature gradients it is useful to report the specific power density as defined in [11] which is $\Gamma = 0.36 nW \cdot cm^{-2} \cdot K^{-2}$. From the slope of the I - V curves shown in Figure 2, it is possible to calculate the electrical resistance (R) of the μTEG , which in this case is mainly dominated by the thermoelectric material. Then, plotting the maximum power for each device at different ΔT versus the electrical resistance (see Figure 2f), it becomes clear the importance of a small electrical resistance in a power generator. The highest output power was obtained for device D4, which has the smallest electrical resistance.

From the slope of the V_{OC} vs ΔT curves in Figure 2 we calculated an average Seebeck coefficient of $S = -135.7 \pm 8.4 \mu V \cdot K^{-1}$ (see Figure S3). The thermal conductance (K) defined as the ratio between the heater power and the temperature gradient obtained, was calculated from the slope of the heater power vs ΔT curve, giving values from 62 to $105 \mu W \cdot K^{-1}$ depending on each device (see Figure S4). Using data from *harvest* and *test* modes, the thermal conductance of the device K_{TEG} can be obtained (see S5 model and discussion).

Each device was also measured in *harvest* mode, by placing the PCB on a hot-plate, with temperatures ranging from 50 to 175 °C. As shown in Figure 3c, the V_{OC} measured in *harvest* mode was significantly lower than in *test* mode. This discrepancy is due to the large thermal resistance of the central part of the membrane and the ambient under natural convection conditions. Since thermal resistance is inversely propor-

tional to the surface area, smaller areas result in greater thermal resistance. For example, when the device D4 was placed on a hotplate at 175 °C, the central part of the membrane reached 151 °C, yielding a temperature gradient of 24 °C across the TE material —16% of the total gradient between the hotplate and room temperature. This thermal bottleneck is irrelevant in *test* mode, where the platform temperature is directly controlled via a heater (see Figure S5 and discussion).

Optimizing thermoelectric harvesting devices requires a multiscale design approach—enhancing not only material properties but also device architecture and system-level thermal management. To improve the performance of the μ TEG, a heat dissipator was mounted on top of the chip, as shown in Figure 3a and 3b. For effective operation, the dissipator must contact only the central regions of the membranes, thereby minimizing thermal resistance to the ambient. To achieve this selective contact, we designed and micromachined custom Si adapters that support the dissipator while minimizing thermal coupling with the hot regions of the device. A similar strategy was previously reported in reference [21]. These adapters consisted of 300 μ m thick Si square plates with a smaller lateral dimension than the chip, each equipped with 5 pillars located on top of each of the central membranes. Additionally, four corner pillars 200 μ m thick, that act as spacers, were included to support the weight of the dissipator and prevent any damage to the membranes.

The dissipator resulted in a 61-fold increase in power output compared to the setup without this thermal management element ($P_{max} = 0.07$ nW vs $P_{max} = 4.28$ nW for $T_{HP} = 175$ °C), as shown in Figure 3c-d). The power output increase reached a factor ca. 110 with the dissipator and under forced air ($1.7 \text{ m}\cdot\text{s}^{-1}$) convection ($P_{max} = 7.75$ nW for $T_{HP} = 175$ °C, see Figure 3e). While thermal management with a dissipator and forced convection provided better results, the power generated in *harvest* mode using this de-

vice architecture still remains approximately seven times lower than in *test* mode, highlighting the importance of thermal management at device level.

A finite element model has been developed to identify possible improvements and compare with experimental results. Figure 4 shows two cases: a) the μ TEG under natural convection; and b) the μ TEG with adapter and dissipator under a forced convection corresponding to air at $1.7\text{m}\cdot\text{s}^{-1}$. The heat exchange coefficient, which defines how much heat is exchanged with the ambient, is set at $h = 10\text{ W}\cdot\text{m}^{-2}\cdot\text{K}^{-1}$ for the natural convection case and $h = 20\text{ W}\cdot\text{m}^{-2}\cdot\text{K}^{-1}$ for the forced convection case. The adapter and dissipator are hidden in the left image of b) to compare the temperature map for both configurations. Both models have a Dirichlet boundary condition applied at the bottom of the μ TEG corresponding to the hotplate temperature and set at $T_{HP} = 100\text{ }^{\circ}\text{C}$, and the air temperature surrounding the device is set at $T_{amb} = 25\text{ }^{\circ}\text{C}$. A thin layer of thermal paste has been added on the contact surfaces between the adapter and the μ TEG (the four corners and five membranes) with a thickness of $10\mu\text{m}$ and a thermal conductivity of $3\text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$ (no pressure is applied in the adapter and dissipator assembly, to minimize the risk of membrane collapse). The maximum power obtained for the D4 device in the model is $P_{max} = 5.29\text{pW}$ for the the μ TEG alone, and $P_{max} = 360.36\text{pW}$ for the μ TEG with adapter and dissipator, resulting in a 68-fold improvement. While the match with experimental results is not quantitative, a similar improvement is obtained when comparing both thermal management options. The main inaccuracies of the model are the convection boundary conditions and the thermal contact between adapter and μ TEG. In addition, it has been identified that some parasitic heat-flow paths from the four corner pillars reach the membrane, reducing its performance. Efforts are now being taken to modify the adapter design, especially the

corner pillars (combining low thermally conducting ceramic materials with silicon microfabricated parts, and reducing the footprint) to enhance the power output.

Combining the different results obtained from electrical conductivity ($\sigma_{Nb:STO} = 1.37 \Omega^{-1} \cdot \text{cm}^{-1}$), thermal conductivity ($\kappa_{Nb:STO} = 3.118 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$) and average Seebeck coefficient ($S_{Nb:STO} = -135.7 \mu\text{V} \cdot \text{K}^{-1}$), we can compute the material power factor and zT , resulting in $PF = 2.52 \mu\text{W} \cdot \text{m}^{-1} \cdot \text{K}^{-2}$ and $zT = 2.43 \cdot 10^{-4}$ at $T = 300 \text{ K}$. Similar calculations can be done for the device ZT . In this case, if we focus on the best performing device (D4), we need the electrical conductance ($G_{D4} = 1/R_{D4} = 3.23 \cdot 10^{-4} \Omega^{-1}$), the thermal conductance ($K_{TEG,D4} = 79.37 \mu\text{W} \cdot \text{K}^{-1}$, see S5) and the Seebeck coefficient ($S_{D4} = -143.2 \mu\text{V} \cdot \text{K}^{-1}$, see Fig S3). The calculated value for $T = 300 \text{ K}$ is $ZT = 2.50 \cdot 10^{-5}$. These results are significantly lower than the state-of-the-art values reported for Nb:STO. While both the thermal conductivity and Seebeck coefficient are consistent with previously reported values, the electrical conductivity measured in our device (as listed in Table 1) is substantially lower than the values reported in the literature for 6% Nb-doped STO [31,33]. This discrepancy may be attributed to the fact that most reported values for Nb:STO are obtained from films grown on lanthanum strontium aluminium tantalate (LSAT) substrates and other crystalline substrates that promote crystalline and epitaxial growth. In contrast, in our case, Nb:STO was deposited onto an amorphous substrate, namely LPCVD-SiN_x, resulting in a non-epitaxial and polycrystalline film. Consequently, its functional properties are degraded due to the distinct microstructural characteristics induced by growth on an amorphous substrate, as opposed to those achieved on substrates optimized for epitaxy and crystallinity. With the integration of appropriate buffer layers (like TiO₂ [34–36] or CeO₂ [37,38]), the electrical conductivity of our TE thin film could potentially match the reported value of $800 \text{ S} \cdot \text{cm}^{-1}$ [32]— corresponding to a 149 nm-thick 6% Nb:STO layer at 300 K. Based on our measured Seebeck coefficient and

thermal resistance, this would translate into a power factor of $S^2 \cdot \sigma = 1.47 \text{ mW} \cdot \text{m}^{-1} \cdot \text{K}^{-2}$, yielding a $zT = 0.142$ and $ZT = 1.46 \cdot 10^{-2}$ at 300 K.

A final comparison with state-of-the art references has been included in Table 2 for the most relevant parameters in terms of μTEG performance. Data from our D4 device are also included for comparison, and a D4* device where the electrical conductivity could reach the $800 \text{ S} \cdot \text{cm}^{-1}$ value. The table shows the relevance of the internal resistance which has a huge impact on the final P_{max} obtained, as well as the impact of a proper architecture which facilitates the heat extraction in microstructures reflected in the final ΔT seen by the thermoelectric material.

Conclusions

Most efforts in the thermoelectric community are focused on optimizing the material zT , and very few are dedicated to thermal management at device (architecture) and system level to improve ZT . In contrast, this work focuses on developing a versatile test platform to evaluate almost any thermoelectric material in thin film form under real operating conditions. While the obtained results do not show an alternative to state-of-the-art thermoelectric devices, they prove the platform flexibility to evaluate the integration of thin film Nb:STO and to evaluate its performance as a μTEG . To the authors knowledge, this work is the first reporting a thin film Nb:STO based μTEG .

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Table 1. Geometric parameters for each of the five different devices on the chip.

	D1	D2	D3	D4	D5
w [μm]	400	300	400	400	500
g [μm]	400	400	600	200	400
$Area = (w+2g)^2$ [mm^2]	1.44	1.21	2.56	0.64	1.69

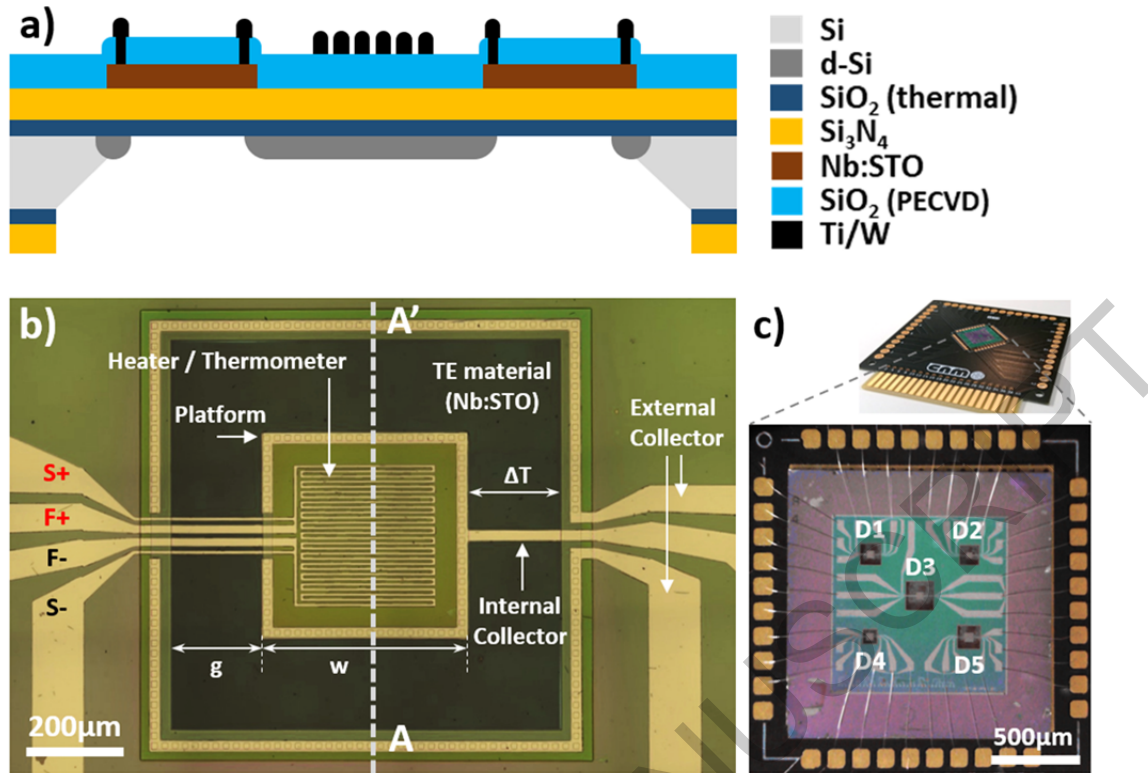


Figure 1: a) Schematic cross section of the μ TEG device corresponding to A-A' in b). b) Optical top view microscope image of a single device (D4). c) Picture of the 1.5x1.5 cm^2 chip mounted on a PCB for thermoelectric characterisation (top) and optical microscope image of a wire-bonded chip showing the five different devices (bottom).

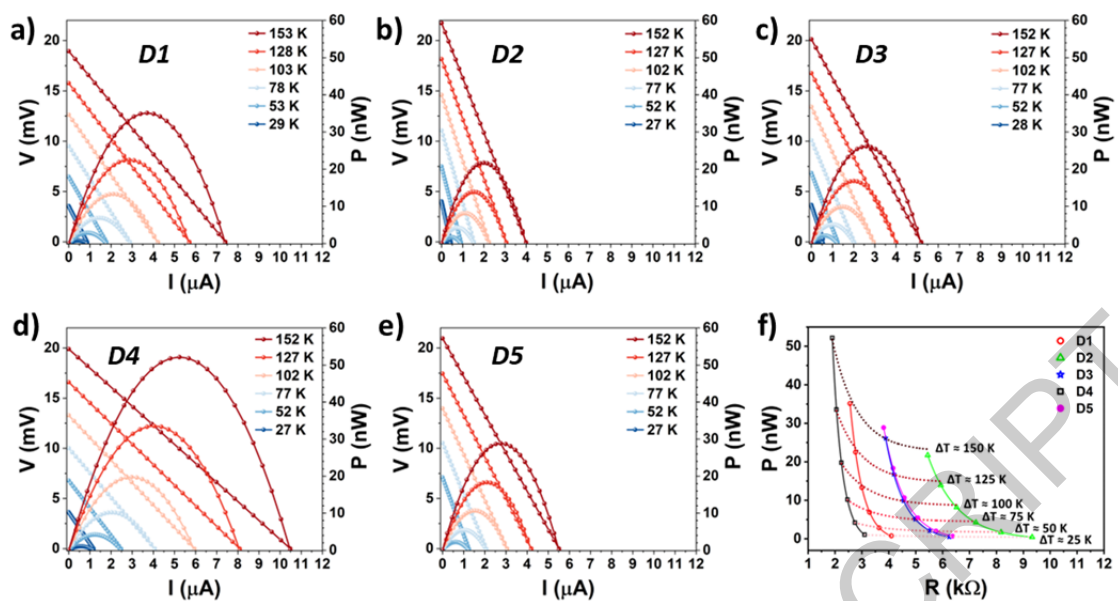


Figure 2. a-e) *test* mode performance plots for the five devices exposed (D1 to D5) to different ΔT . f) Influence of electric resistance on the maximum power generated by the five devices at different ΔT . All ΔT reported are relative to room temperature $T_{amb}=25^{\circ}\text{C}$.

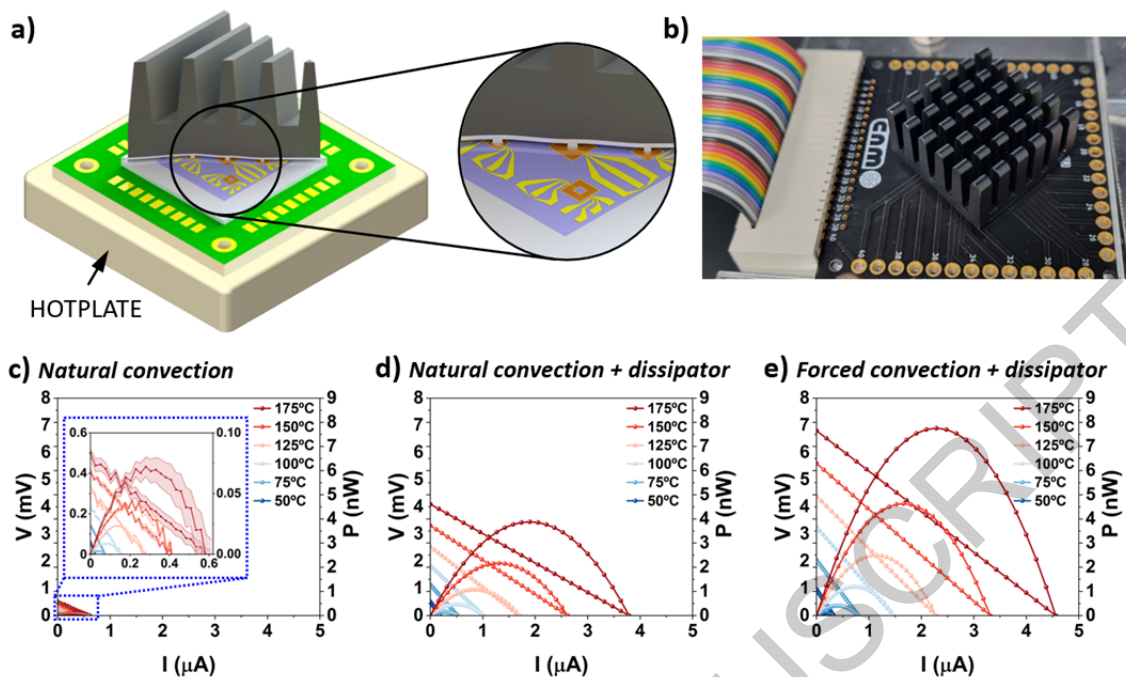


Figure 3: a) Scheme of the dissipator mounting strategy by using an intermediate adapter for harvest mode measurements and placing the PCB on top of a hotplate. b) Image of the PCB containing the chip with adapter and dissipator on top. Performance plots in *harvest* mode for the device D4 with different thermal management configurations, with hot-plate temperatures from 50 °C to 175 °C, under c) natural convection, d) natural convection with dissipator, and e) forced convection with dissipator.

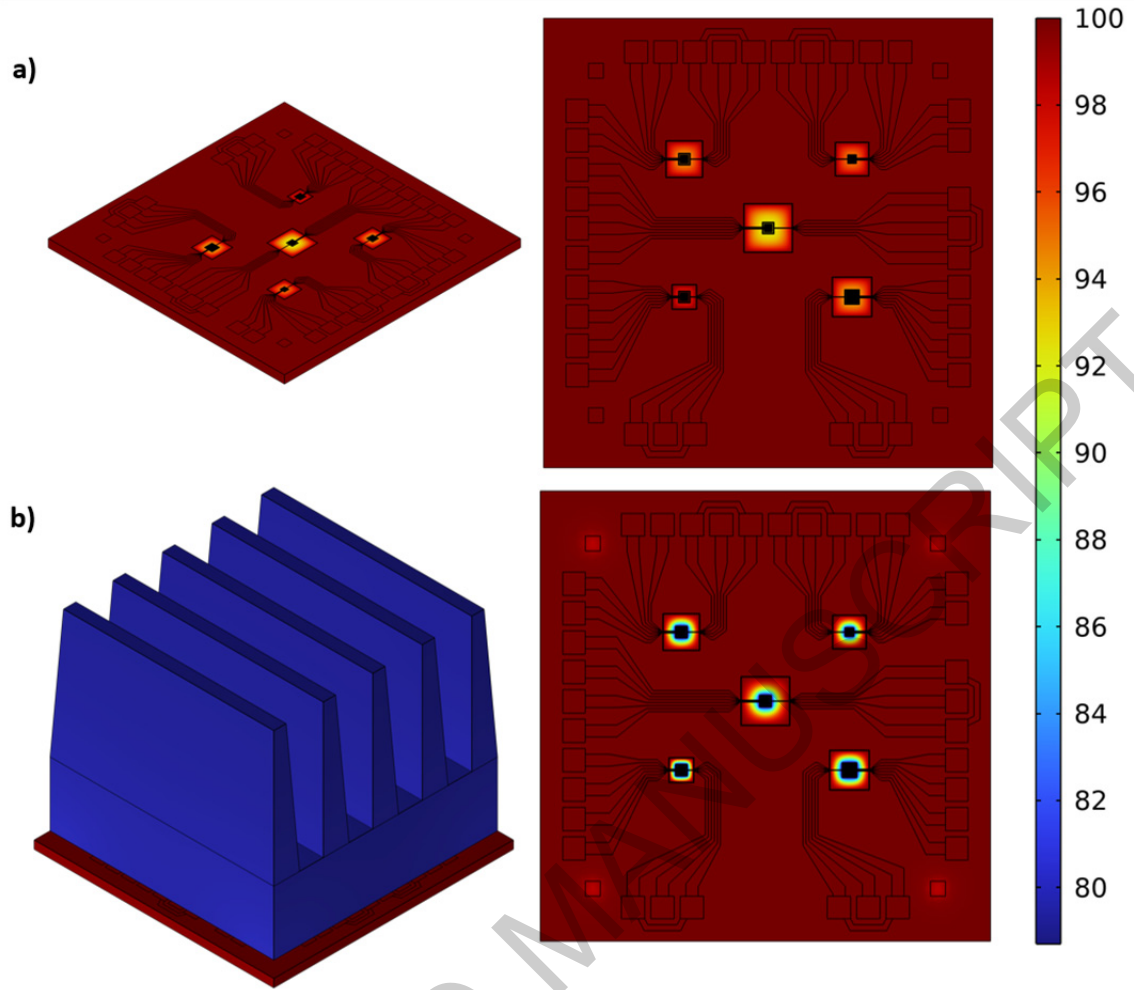
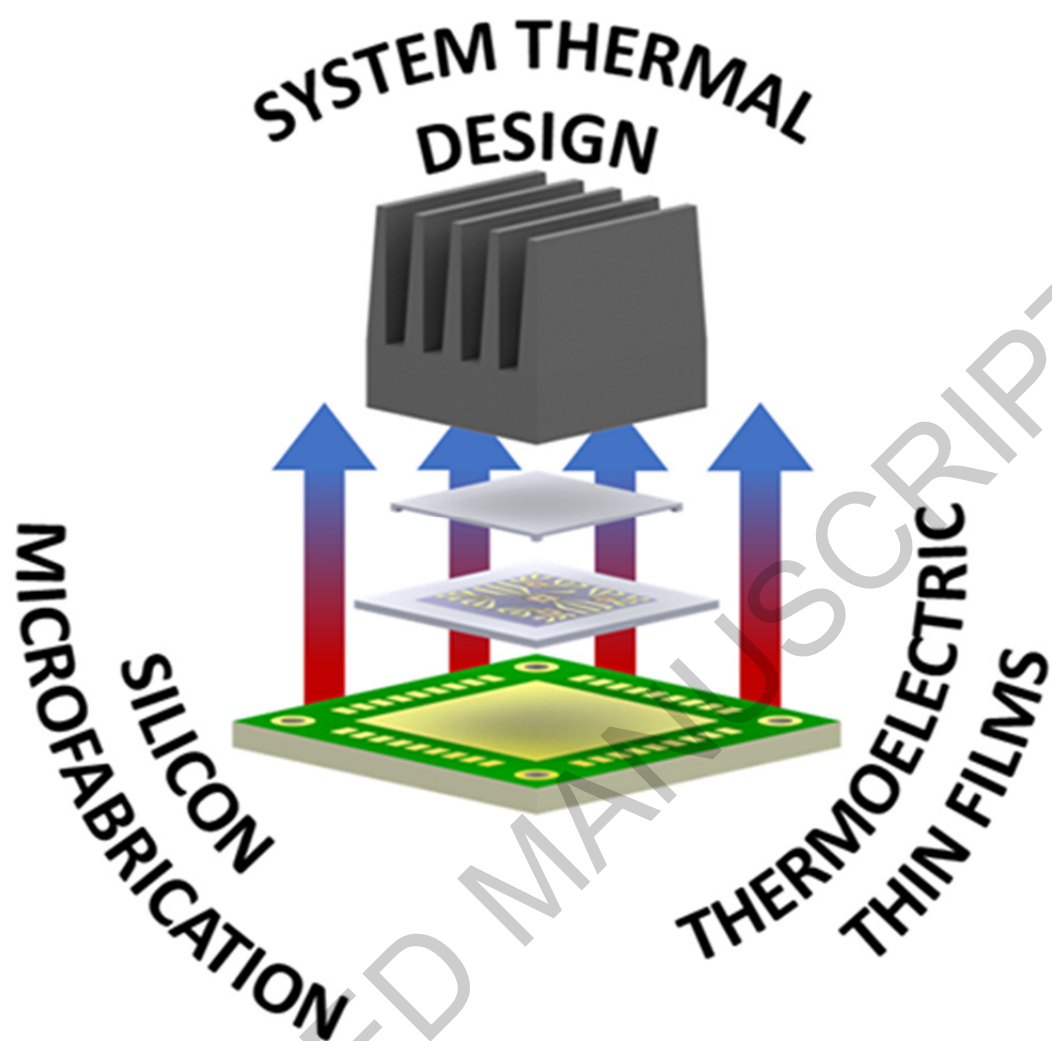


Figure 4: Temperature (in °C) results of the finite element model (COMSOL) corresponding to a) the μ TEG in natural convection with heat exchange coefficient $h = 10 \text{ W} \cdot \text{m}^{-2} \cdot \text{K}^{-1}$ and b) the μ TEG with adapter and heat dissipator under forced convection with $h = 20 \text{ W} \cdot \text{m}^{-2} \cdot \text{K}^{-1}$, corresponding to an air velocity of $1.7 \text{ m} \cdot \text{s}^{-1}$. A temperature of $T_{HP} = 100 \text{ }^{\circ}\text{C}$ is set at the bottom of the model to account for the hotplate temperature and $T_{amb} = 25^{\circ}\text{C}$.

Table 2. Comparison with state-of-the-art references with D4 device for most relevant parameters for μ TEG performance. Where available, ZT and zT are evaluated at 300K. All values found in the references are in bold, while those in italics are calculated from data in the references. D4* corresponds to the D4 device assuming an electrical conductivity of $800 \text{ S}\cdot\text{cm}^{-1}$ instead of the obtained one of $1.37 \text{ S}\cdot\text{cm}^{-1}$.

Ref	Γ $\mu\text{W}\cdot\text{cm}^{-2}\cdot\text{K}^{-2}$	P_{dens} $\mu\text{W}\cdot\text{cm}^{-2}$	R_{int} Ω	zT/ZT	footprint cm^2	ΔT (condition) K
[11]	0.052	1.3	52.8e6	-/-	1	5 (forced)
[21]	6.4e-3	<i>67.45</i>	<i>51.04</i>	-/-	0.49	49.5 ($T_{\text{HP}}=200^\circ\text{C}$)
[22]	1.3	100	38.8	0.02/0.016	0.077	10 ($\text{RT}+10^\circ\text{C}$)
D4	3.6e-4	1.21	3096	2.4e-4/2.5e-5	6.4e-3	<i>46.1</i> <i>($T_{\text{HP}}=175^\circ\text{C}$)</i>
D4*	<i>0.21</i>	<i>707.1</i>	<i>5.302</i>	<i>0.142/0.0146</i>	6.4e-3	<i>46.1</i> <i>($T_{\text{HP}}=175^\circ\text{C}$)</i>



GraphicalAbstract1

Supplementary Information

A novel approach to micro-fabricated thermoelectric generators with SrTiO₃

Joaquin Santander^a, Iñigo Martin-Fernandez^a, Carlos Carbonell^a, Alex Rodríguez-Iglesias^a, Laura Fuentes-Rodríguez^a, Marta Fernández-Regúlez^a, Llibertat Abad^a, Aitor F. Lopeandia^{b,c}, Arindom Chatterjee^d, Nini Pryds^d, Luis Fonseca^a, and Marc Salleras^{a*}

^a*Institute of Microelectronics of Barcelona (IMB-CNM-CSIC), 08193 Bellaterra, Spain.*

^b*Physics Department, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain.*

^c*GTNAM at Institut Català de Nanociència i Nanotecnologia (ICN2), 08193 Bellaterra, Spain.*

^d*Department of Energy Conversion and Storage, Technical University of Denmark, 2800 Kgs Lyngby, Denmark.*

*marc.salleras@csic.es

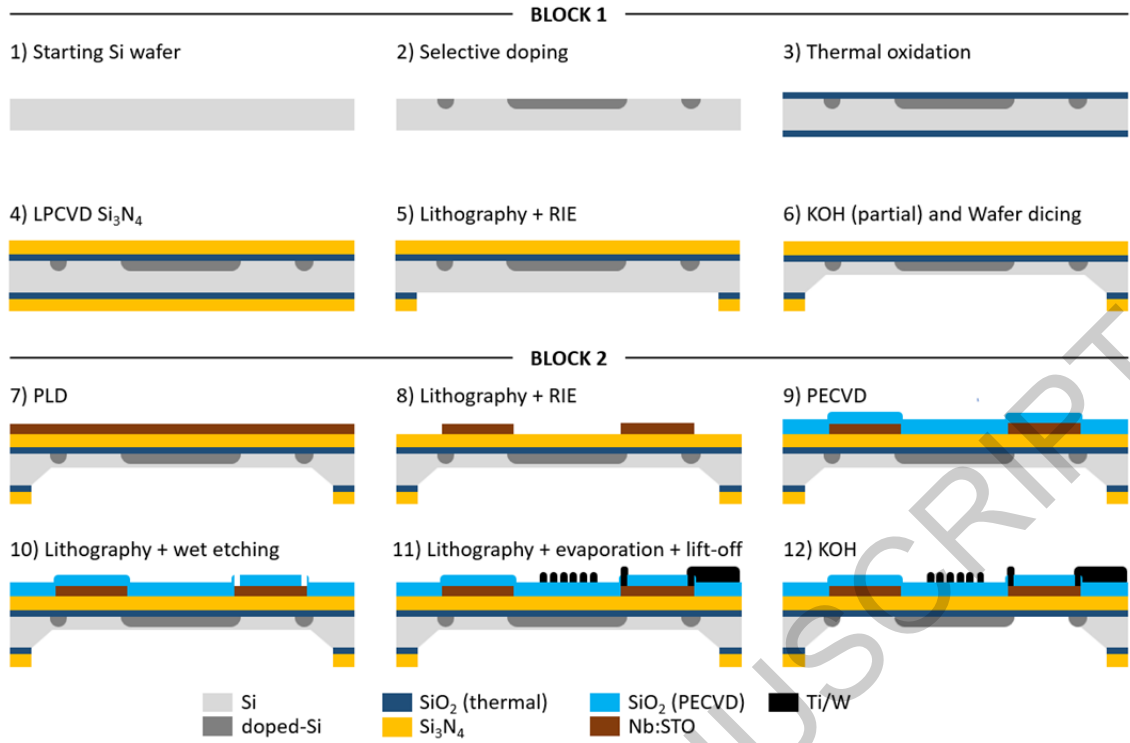


Figure S1: Schematics of the fabrication scheme. The fabrication is divided in 2 blocks. Block 1 comprises the process steps at a wafer-scale level. Block 2 comprises the process steps at a chip-scale level. (1) Starting wafers; (2) Selective doping of Si with BBr₃; (3) Growth of 100 nm SiO₂ by thermal oxidation (4) deposition of low stress Si₃N₄ by LPCVD; (5) Optical lithography followed by RIE and photoresist removal to pattern the membrane windows; (6) Partial wet etch with KOH of the Si and wafer dicing into chips; (7) PLD deposition of the Nb:STO; (8) Optical lithography followed by Ar plasma and photoresist removal to pattern the Nb:STO; (9) PECVD deposition of 200 nm SiO₂ as interlevel oxide; (10) Optical lithography, wet etching, and photoresist removal to define the bias to the Nb:STO; (11) Optical lithography, evaporation of 10 nm Ti and 200 nm W and lift-off to pattern the current collectors and the heaters, the tracks and the metal pads; and (12) Complete KOH etching of the Si to define the membranes.

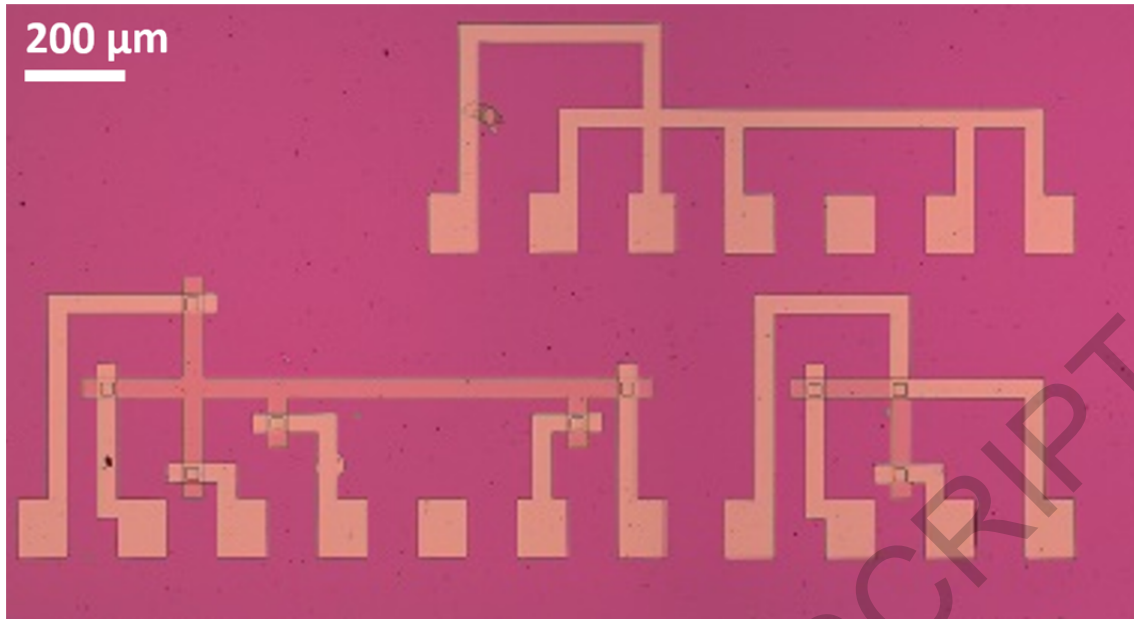


Figure S2. Test structures used for the measurement of electrical parameters.

The chips include a set of electrical test structures able to measure basic electrical technological parameters like the sheet resistance of conducting layers (Van der Pauw test structures, lower left image in Figure S2) and the contact resistance between conducting layers (Kelvin test structure, lower right image in Figure S2). Table S1 summarizes the obtained values, which confirm that the chips were fabricated as expected. The value of the sheet resistance of the Nb:STO permits the calculation of the electrical conductance provided the thickness of the layer (149 nm).

Table S1. Measurements obtained for the technological parameters: sheet resistances of the metal and of the Nb:STO layers and contact resistance between the metal and the Nb:STO layers in a $20 \times 20 \mu\text{m}^2$ contact area.

R_{\square} metal	$1.3 \Omega/\square$
R_{\square} Nb:STO	$49 \text{ k}\Omega/\square$
R_c metal to Nb:STO	$1.7 \text{ k}\Omega$

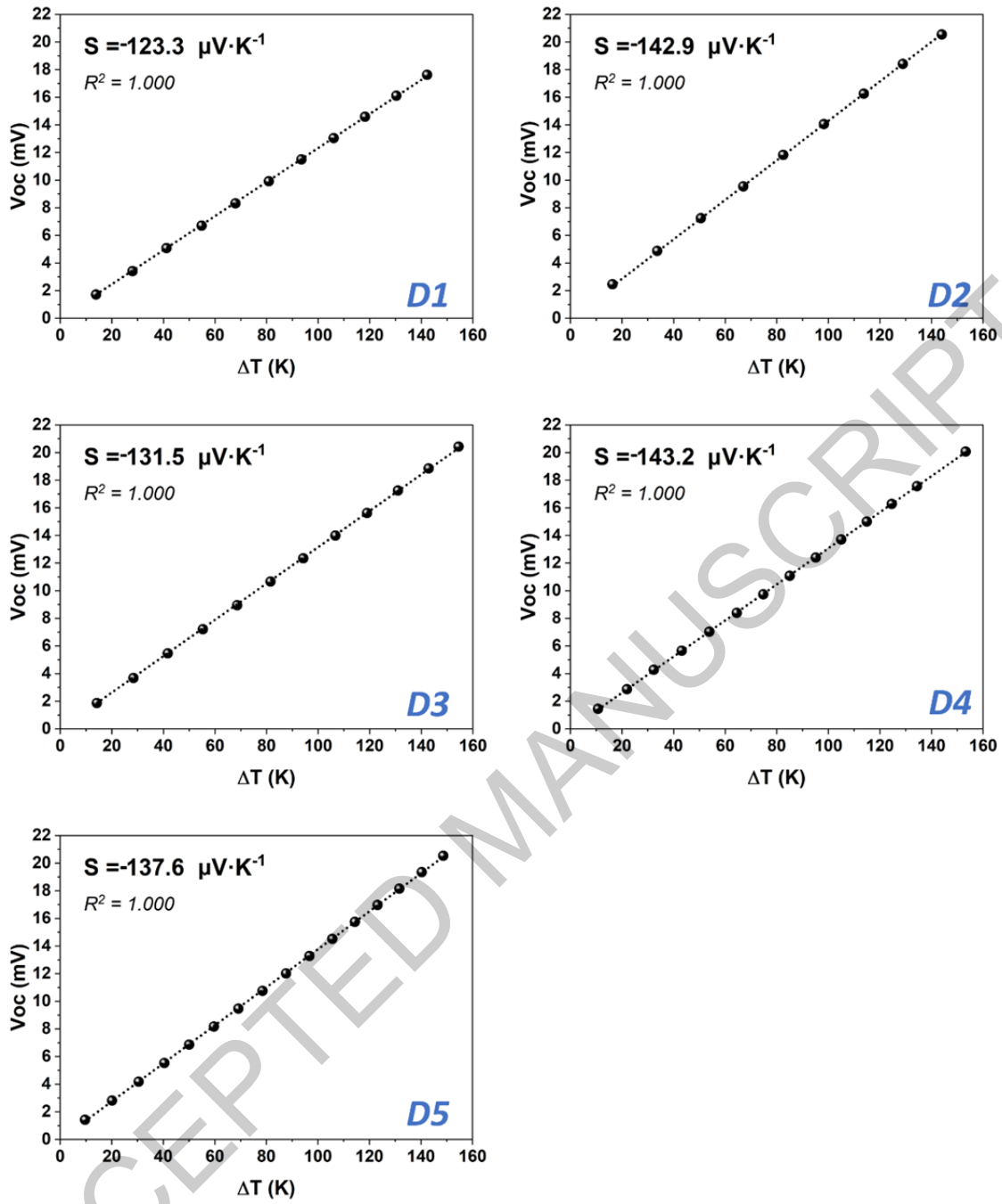


Figure S3. Determination of the Seebeck coefficient (S) for each of the five devices from the slope of the V_{OC} vs ΔT curves. The average is $S = -135.7 \pm 8.4 \mu V \cdot K^{-1}$.

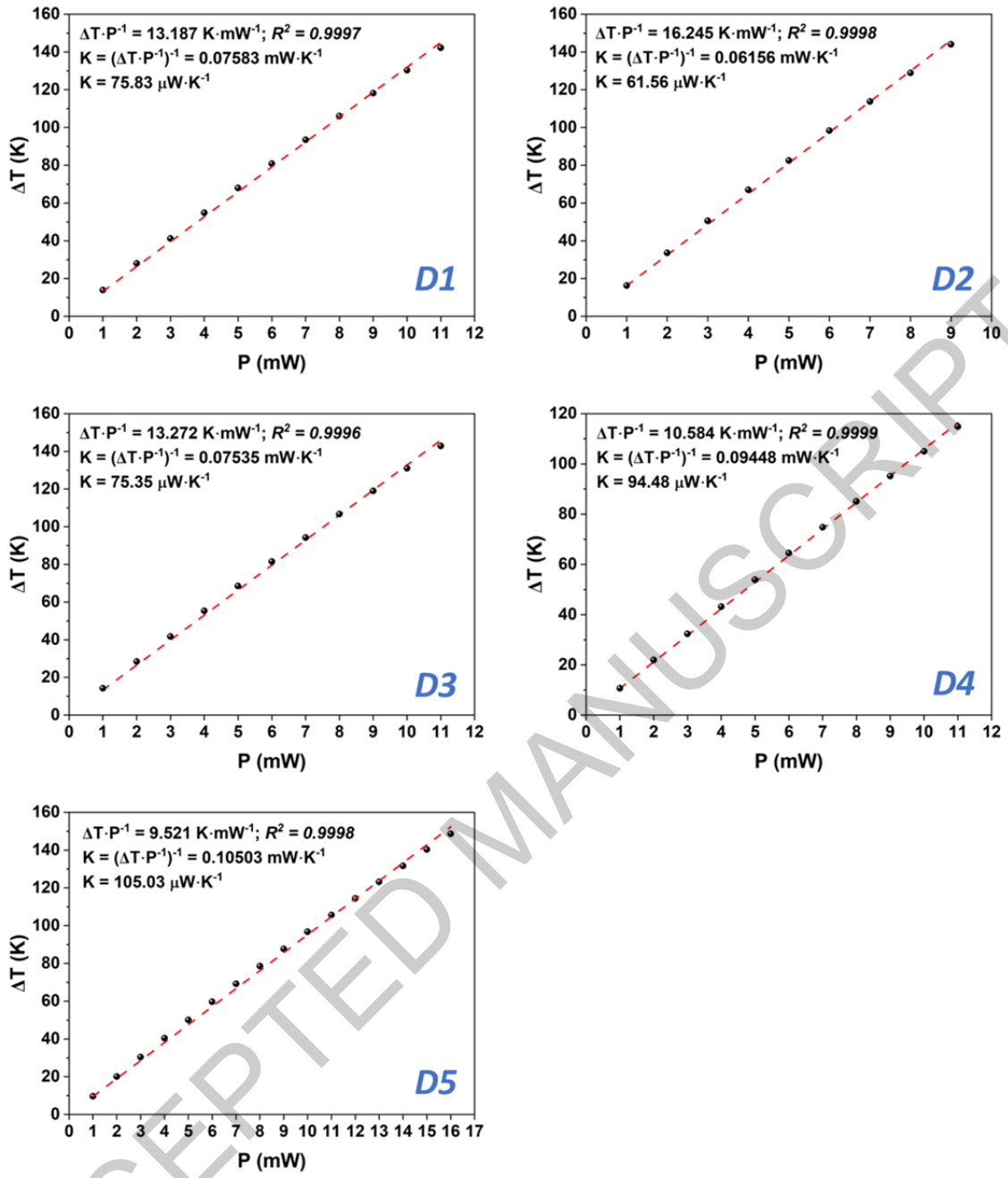


Figure S4. Determination of the thermal conductance (K) of the five devices from the slope of the ΔT vs heater power curves.

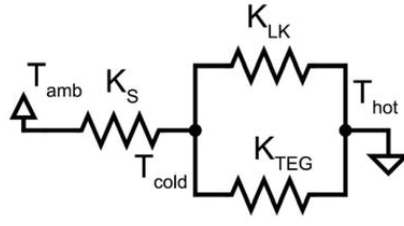


Figure S5: Simplified thermal model of the μ TEG.

In the calculation of the thermal conductance of the TEG (K_{TEG}) the simple thermal model in Figure S5 is used. In this model the node T_{cold} is where the heater/thermometer is placed and T_{hot} is the hotplate. K_{TEG} is the thermal conductance of the device (the thermoelectric membrane), K_{LK} is the leakage thermal conductance (through parasitic heat-flow paths), and K_S is the thermal conductance from the heater/thermometer towards the ambient.

For this discussion, we will focus on D4 device and will ignore the K_{LK} term as it is expected to be much smaller than K_{TEG} . From our *test* mode results, we can calculate the thermal conductance from the slope of ΔT vs heater power curves (Figure S4) resulting in $K_{D4} = 94.48 \mu W \cdot K^{-1}$. According to the thermal model, this thermal conductance corresponds to the parallel connection of K_{TEG} and K_S , therefore $K_{D4} = K_{TEG,D4} + K_{S,D4}$. In *harvest* mode we set the hotplate temperature at 175 °C, and the heater (used as a thermometer) measures a temperature of 151 °C, while the ambient temperature measured is 25 °C. Then we can calculate for D4:

$$Q = dT \cdot K \rightarrow Q = (175 - 151 \text{ } ^\circ\text{C}) \cdot K_{TEG} = (151 - 25 \text{ } ^\circ\text{C}) \cdot K_S$$

$$24 \text{ } ^\circ\text{C} \cdot K_{TEG} = 126 \text{ } ^\circ\text{C} \cdot K_S \rightarrow K_{TEG} = 126/24 \cdot K_S = 5.25 \cdot K_S$$

And using: $K_{TEG} + K_S = 94.48 \mu W \cdot K^{-1}$

We can obtain: $K_{TEG} = 79.37 \mu W \cdot K^{-1} \rightarrow K_S = 15.12 \mu W \cdot K^{-1}$

The K_{TEG} value obtained can be used to calculate a ZT value.

ACCEPTED MANUSCRIPT